**Shubham Kumar Tiwari**

**PROFILE**

A technically astute and diligent M. Tech Scholar with specialization in VLSI Design. Seeking to achieve high career growth through a continuous learning process, persist in being dynamic, visionary, and competitive with changing scenarios of the world and contribute to the success of the organization.

**EDUCATION**

* **M.Tech** **VLSI Design**

**CGPA – 8.57 / 10**

Amrita Vishwa Vidyapeetham

* **B.Tech** **Electronics and Communication Engineering**

**CGPA – 8.51 / 10**

IET, M. J. P. Rohilkhand University, Bareilly.

* **Class 12** – 90.4%

Institution:

* **Class 10** – 87.16%

Institution:

**TECHNICAL INTERESTS**

VLSI Design

**PROJECTS**

**An Efficient Side-Channel Analysis Based Approach to Detect Hardware Trojans**

This work focuses on the side-channel analysis method based on path delay measurement for detecting hardware Trojans inside the circuit. Identified and observed the paths where Trojans have an impact. The other side-channel parameters considered for comparison are power

consumption and area utilization. 

**Design and Verification of a UART**

The UART protocol has been designed, and its functional verification was done through the implementation of verification environment, which includes component such as transactor, generator, driver, monitor, interface, and scoreboard.

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| **Design and implementation of Router 1×3 using Xilinx Vivado.** | |
| The work focus on designing a router in which, the data |
| packets are transmitted to three networks.  **Design and Simulation of Phase Looked Loop (UG Project).** | |

The focus of the work is on designing a PLL system using 90nm process technology (PTM 90nm) with Symica DE Analog Design Environment. The current starved ring oscillator was considered here for its superior performance and its VCO design providing 2.54GHz at 0.9V (control voltage) and Kvco (VCO gain) of 3.56GHz/V.

**TECHNICAL SKILLS**

HDL/HVL: Verilog and SystemVerilog

Other Programming Languages: Python and Basic C++.

Basic knowledge of Python Scripting.

Protocols: UART, I2C, SPI and AXI. 

EDA Tool: ModelSim, Quartus Prime, Xilinx Vivado,

Synopsys Protocompiler, and Synopsys Synplify.

Knowledge of Digital Electronics.

**INTERNSHIP**

**Synopsys (India) Pvt. Ltd.,** *RMZ Infinity, Bangalore* Joined as a Graduate Engineer Trainee in the System Design Group, which primarily works on the prototyping of ASIC designs. Prototyping is done on the ProtoCompiler tool, the Synplify tool and HAPS-100 hardware.

I worked on the design of a simulation environment

for the RISC-V processor, where I was assigned to

create the script for dumping the hex and binary

value for the C code, which can be written to the DDR4, and helped in verifying the disassembler design to convert the binary value to assembly

language. Also handled debugging of the AXI

transaction between RISCV and DDR4.

**Summer Training in VLSI Design field using Verilog and FPGA at DKOP LABS PVT. LTD.**

2 MONTHS NOIDA

**CERTIFICATIONS**

**SOC Verification using SystemVerilog from Udemy.**

**System Design using Verilog from Udemy.**

**ACHIEVEMENTS & HONOURS**

Awarded as a Gold medallist for my overall performance in Bachelor of Technology (ECE).

**LANGUAGES**

English, Hindi